ABSTRACT OF THE DISCLOSURE

A layer defining unit defines different layer numbers to oblique wiring diagrams and via cell diagrams which are included in layout data of a semiconductor integrated circuit design. A first diagram blending unit fetches diagram data including the oblique wiring diagrams and the via cell diagrams from the layout data, synthesizes the diagrams every same layer number, and blends them in overlapped portions. An oblique wiring verifying unit verifies an interval between the oblique wiring diagrams blended by the first diagram blending unit by an allowable minimum interval value S. A second diagram blending unit synthesizes the verified oblique wiring diagram and the via mat diagram of the via cell, thereby forming an oblique wiring mask diagram blended in an overlapped portion. A blended diagram verifying unit verifies an interval between the oblique wirings having projecting portions by the via cells of the oblique wiring mask diagram blended by the second diagram blending unit by an allowable minimum interval value T (where, $T < S$).